

A Class of Irregular LDPC Codes with Low Error Floor and Low Encoding Complexity

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Abstract—In this letter, we propose a class of irregular structured low-density parity-check (LDPC) codes with low error floor and low encoding complexity by designing the parity check matrix in a triangular plus dual-diagonal form. The proposed irregular codes clearly lower the error floor and dramatically improve the performance in the waterfall region of error-rate curves. Being characterized by linear encoding complexity, the encoders of the proposed codes attain throughputs over 10 Gbit/s.

Index Terms—Low density parity check codes, error floor, linear encoding.

I. INTRODUCTION

STRUCTURED low-density parity-check (LDPC) codes constructed from circulant permutation matrices have recently received a lot of interest (e.g., [1] - [3]) because of their simple structures which dramatically reduce the storage requirements associated with the parity check matrix in encoders and decoders. By choosing proper degree distributions, irregular LDPC codes with non-constant column degrees and non-constant row degrees which outperform regular LDPC codes are capable of transmitting information over noisy channels with a capacity close to the Shannon limit [3] - [9].

In this letter, we propose an efficient approach to the design of high-performance irregular structured LDPC codes based on circulant permutation matrices with a bit-error-rate (BER) floor below 10^{-9} . Since the parity check matrix has a triangular plus dual-diagonal form, the proposed codes can be encoded with the same low encoding complexity as repeat-accumulate codes (e.g. [9]). The encoders attain throughputs of more than 10 Gbit/s by using only several hundred exclusive-OR (XOR) gates. They are suitable for high-speed applications in the Gbit/s region, such as long-haul optical channels and Gigabit Ethernet.

II. CODE CONSTRUCTION

We propose a class of irregular LDPC code represented by the following parity-check matrix $\mathbf{H} = [\mathbf{H}_S | \mathbf{H}_P]$ in which each column and each row have non-constant degrees, i.e.

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$$\mathbf{H}_S = \begin{bmatrix} \mathbf{H}_{1,1} & \cdots & \mathbf{H}_{1,L-J} \\ \vdots & \ddots & \vdots \\ \mathbf{H}_{J-1,1} & \cdots & \mathbf{H}_{J-1,L-J} \\ \mathbf{H}_{J,1} & \cdots & \mathbf{H}_{J,L-J} \end{bmatrix}, \quad (1)$$

$$\mathbf{H}_P = \begin{bmatrix} \mathbf{I} & \cdots & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ \mathbf{H}_{J-1,L-J+1} & \cdots & \mathbf{H}_{J-1,L-2} & \mathbf{I} & \mathbf{I}(q-1) \\ \mathbf{H}_{J,L-J+1} & \cdots & \mathbf{H}_{J,L-2} & \mathbf{I} & \mathbf{I} \end{bmatrix}, \quad (2)$$

where $\mathbf{0}$ and \mathbf{I} are the $q \times q$ null matrix and the identity matrix, respectively, and $\mathbf{I}(q-1)$ is a $q \times q$ circulant matrix obtained by circulating the rows of \mathbf{I} to the right by $(q-1)$ places. For $1 \leq j \leq J$ and $1 \leq l \leq L$, the sub-matrix $\mathbf{H}_{j,l}$ in position (j,l) within \mathbf{H} is either a null matrix or a circulant matrix obtained by circulating the rows of \mathbf{I} to the right by $C_{j,l}$ places, i.e. $\mathbf{H}_{j,l} \equiv \mathbf{I}(C_{j,l})$. The code defined by \mathbf{H} has a block length of $n = q \times L$ and a code rate of $R = (1 - J/L)$. The shifting coefficient $C_{j,l}$ is chosen randomly in such a way as to avoid short cycles in the code's Tanner graph. To avoid the $2i$ -cycle, a necessary and sufficient condition is [2]

$$\sum_{k=1}^m (C_{j_k, l_k} - C_{j_{k+1}, l_k}) \neq 0 \pmod{q}, \quad (3)$$

for all m , $2 \leq m \leq i$, all j_k , $1 \leq j_k \leq J$, all j_{k+1} , $1 \leq j_{k+1} \leq J$, and all l_k , $1 \leq l_k \leq L$, with $j_0 = j_m$.

An important contribution in this letter is that four sub-matrices which compose a dual-diagonal matrix are used at the lower-right corner of \mathbf{H}_P to lower the error floor and reduce encoding complexity. To illustrate why the four sub-matrices $\begin{bmatrix} \mathbf{I} & \mathbf{I}(q-1) \\ \mathbf{I} & \mathbf{I} \end{bmatrix}$ can compose a dual-diagonal matrix, Fig. 1(a) shows an 8×8 dual-diagonal matrix which is reorganized into four 4×4 sub-matrices, where the top (bottom) two sub-matrices are constructed from the odd (even) rows of the dual-diagonal matrix. Thus, by putting the rows of $\mathbf{H}_{J-1} = [\mathbf{H}_{J-1,1} \cdots \mathbf{H}_{J-1,L-2} \quad \mathbf{I} \quad \mathbf{I}(q-1)]$ and $\mathbf{H}_J = [\mathbf{H}_{J,1} \cdots \mathbf{H}_{J,L-2} \quad \mathbf{I} \quad \mathbf{I}]$ into the odd and even rows of \mathbf{H} , respectively, the proposed matrix has a triangular plus dual-diagonal form. Please note that a one in position $(1, 4)$ within $\mathbf{I}(3)$ is replaced by a zero to construct a dual-diagonal matrix in Fig. 1(a). Fig. 1(b) shows an intuitive example of \mathbf{H} , where the four rows of \mathbf{H}_2 are put in rows 5, 7, 9, 11 and the four rows of \mathbf{H}_3 are put into rows 6, 8, 10, 12 in \mathbf{H} . Section IV describes precisely how the rows of \mathbf{H}_{J-1} and \mathbf{H}_J are positioned in \mathbf{H} .

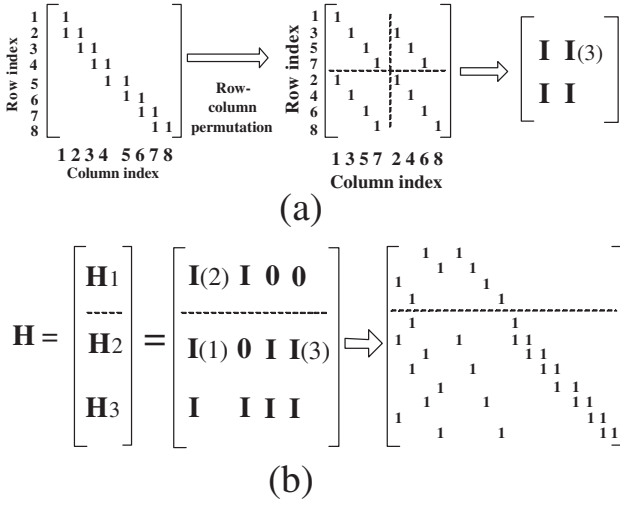


Fig. 1. (a) A dual-diagonal matrix composed of four sub-matrices; (b) the proposed matrix in a triangle plus dual-diagonal form.

III. LOW ERROR FLOOR

Based on extensive numerical simulations, we have found that both the degree distributions and the shifting coefficients of \mathbf{H} affect the error floor. The following approaches are suggested to lower the error floors of irregular LDPC codes.

1) *Degree distributions*: The columns with large degrees should be put into \mathbf{H}_S where no column of degree 2 or 1 is allowed. Instead of the triangular form or the dual-diagonal form, \mathbf{H}_P is given a triangular plus dual-diagonal form to increase the minimum distance.

2) *Shifting coefficient*: The shifting coefficients are chosen starting from the columns with low degrees to the columns with high degrees, i.e. the coefficients for columns with degrees 2 and 3 are chosen by avoiding short cycles and cycles of medium length during the design procedure. Then the coefficients for columns with degree above 3 are chosen by avoiding short cycles.

As an example, consider irregular codes with a q value of 128, a block length of 2048, and a code rate of 1/2. The matrix $\mathbf{H} = [\mathbf{H}_S | \mathbf{H}_P]$ shown in Fig. 2 has degree distributions $\lambda_2 = 0.375$, $\lambda_3 = 0.5$, and $\lambda_8 = 0.125$, where λ_i denotes the fraction of columns with degree i in \mathbf{H} . The shifting coefficients for columns with degrees 2 and 3 were chosen randomly from the rightmost column to the leftmost column with the constraint which avoids cycles of length 4, 6, and 8. Then, the coefficients for columns with degree 8 are chosen by avoiding cycles of lengths 4 and 6. The bit error rate (BER) of three irregular LDPC codes versus the signal-to-noise ratio (SNR) per bit E_b/N_0 are shown in Fig. 3, assuming binary phase-shift keying (BPSK) modulation and an AWGN channel. The iterative belief-propagation algorithm with a maximum of 200 iterations was used for decoding. The so-called triangular code in Fig. 3 is the irregular LDPC code obtained by substituting a null sub-matrix for the sub-matrix $\mathbf{I}(127)$ in position (7, 8) within \mathbf{H}_P , while the so-called dual-diagonal code is the code obtained by substituting two null sub-matrices for the sub-matrices $\mathbf{I}(21)$ in position (6, 1) and $\mathbf{I}(10)$ in position (8, 2) within \mathbf{H}_P .

$$\mathbf{H}_S = \begin{bmatrix} \mathbf{I}(46) & \mathbf{I}(64) & \mathbf{I}(85) & \mathbf{I}(24) & \mathbf{I}(106) & \mathbf{I}(59) \\ & \mathbf{I}(14) & \mathbf{I}(69) & & \mathbf{I}(105) & \mathbf{I}(108) \\ & & \mathbf{I}(111) & \mathbf{I}(54) & & \mathbf{I}(34) & \mathbf{I}(31) \\ \mathbf{I}(112) & \mathbf{I}(119) & & \mathbf{I}(22) & & \mathbf{I}(36) \\ & \mathbf{I}(18) & \mathbf{I}(56) & & \mathbf{I}(104) & \mathbf{I}(36) \\ & & \mathbf{I}(2) & \mathbf{I}(15) & \mathbf{I}(92) & \mathbf{I}(106) \\ \mathbf{I} & \mathbf{I}(107) & & & & \mathbf{I}(10) & \mathbf{I}(56) \\ & \mathbf{I}(112) & \mathbf{I}(6) & & \mathbf{I}(20) & & \mathbf{I}(123) \end{bmatrix}$$

$$\mathbf{H}_P = \begin{bmatrix} \mathbf{I} \\ \mathbf{I}(59) & \mathbf{I} \\ & \mathbf{I}(63) & \mathbf{I} \\ & & \mathbf{I}(20) & \mathbf{I} \\ & & & \mathbf{I}(75) & \mathbf{I} \\ \mathbf{I}(21) & & & \mathbf{I}(67) & \mathbf{I} \\ & & & & \mathbf{I}(72) & \mathbf{I} & \mathbf{I}(127) \\ & \mathbf{I}(10) & & & & \mathbf{I} & \mathbf{I} \end{bmatrix}$$

Fig. 2. Parity-check matrix $\mathbf{H} = [\mathbf{H}_S | \mathbf{H}_P]$ of an irregular LDPC code. Unmarked spaces are null sub-matrices.

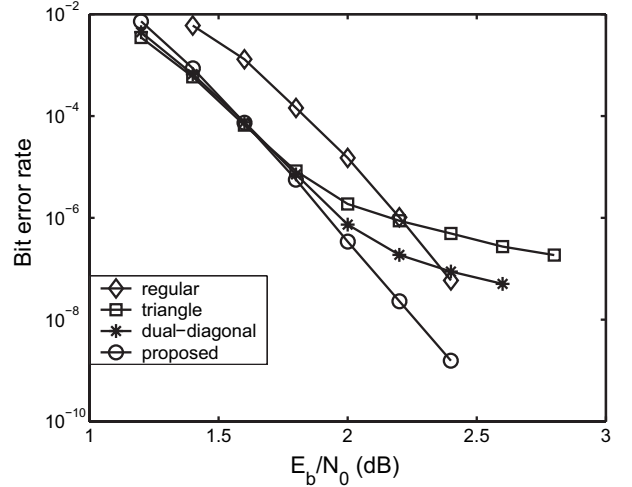


Fig. 3. BER comparison of three irregular codes with a code rate of 1/2 and a block length of 2048. The regular code has a column degree of 4.

The proposed irregular codes clearly lower the error floor and dramatically improve the performance in the waterfall region of the BER curves. Though error floors at 10^{-6} and 10^{-7} are observed for the irregular codes with a triangular matrix and a dual-diagonal matrix, respectively, the error floor of the proposed irregular code is below 10^{-9} . To estimate the minimum distances of the codes which affect the error floors, the following table lists the distances d_1 , d_2 , d_3 , and d_4 , where d_i is the minimum weight of the codeword when the weight of the systematic part is i . The minimum distances of the irregular codes with a triangular matrix, a dual-diagonal matrix, and the proposed matrix are upper-bounded at 13, 14 and 22, respectively.

TABLE I
MINIMUM DISTANCES OF THREE IRREGULAR CODES

	d_1	d_2	d_3	d_4	Minimum distance
Triangular	14	13	14	15	≤ 13
Dual-diagonal	14	22	16	22	≤ 14
Proposed	25	24	23	22	≤ 22

For comparison purposes, the BER performance of a regular LDPC code with a column degree of 4, a row degree of 8, a block length of 2048 and a code rate of 1/2 is also shown in Fig. 3. Though the regular code has good performance in the error floor region, it exhibits a 0.2 dB loss with respect to the proposed irregular code.

IV. LINEAR ENCODING

Since LDPC codes are linear codes, \mathbf{x} is a codeword if and only if

$$\mathbf{H} \mathbf{x}^T = \mathbf{0}^T \quad (4)$$

Consider a partitioning of \mathbf{x} into $(J + 1)$ parts, i.e. $\mathbf{x} = (\mathbf{u}, \mathbf{p}_1, \dots, \mathbf{p}_J)$, where \mathbf{u} denotes the systematic part and $(\mathbf{p}_1, \dots, \mathbf{p}_J)$ denote the parity parts. Since \mathbf{H} has a triangular plus dual-diagonal form, the above equation is naturally broken down as follows:

$$p_j(i) = \sum_{k=1}^{L-J} g_{j,k} u(a_{j,k,i}) + \sum_{k=1}^{j-1} g_{j,k} p_k(b_{j, L-J+k, i}), \quad (5)$$

$$p_{J-1}(i) = v(i) + p_{J-1}(i-1), \quad (6)$$

$$p_J(i) = v(i+q) + p_J(i-1), \quad (7)$$

for all i , $1 \leq i \leq q$, and for all j , $1 \leq j \leq J-2$, where $p_{J-1}(0) = 0$ and $p_J(0) = p_{J-1}(q)$, and the intermediate vector \mathbf{v} is given by

$$v(2i-1) = \sum_{k=1}^{L-J} g_{J-1,k} u(a_{J-1,k,i}) + \sum_{k=1}^{J-2} g_{J-1,k} p_k(b_{J-1, L-J+k, i}), \quad (8)$$

$$v(2i) = \sum_{k=1}^{L-J} g_{J,k} u(a_{J,k,i}) + \sum_{k=1}^{J-2} g_{J,k} p_k(b_{J, L-J+k, i}), \quad (9)$$

The indices $a_{j,k,i}$ of vector \mathbf{u} and the indices $b_{j,L-J+k,i}$ of vector \mathbf{p}_k are defined as:

$$a_{j,k,i} = [i + C_{j,k}]_q + (k-1) \times q, \quad (10)$$

$$b_{j,L-J+k,i} = [i + C_{j,L-J+k}]_q + (k-1) \times q, \quad (11)$$

where $[x]_q$ denotes x modulo- q arithmetic. The coefficients $g_{j,k}$ in (5), (8), and (9) are defined as:

$$g_{j,k} = \begin{cases} 1, & \text{when } \mathbf{H}_{j,k} = \mathbf{I}(C_{j,k}), \\ 0, & \text{when } \mathbf{H}_{j,k} = \mathbf{0}, \end{cases} \quad (12)$$

for all j , $1 \leq j \leq J$, and for all k , $1 \leq k \leq L-2$.

We implemented an encoder for the proposed LDPC code with a q value of 128, a block length of 2048, and a code rate of 1/2 into Xilinx Virtex-II Field Programmable Gate Array (FPGA) devices. The systematic bits \mathbf{u} and the parity bits $(\mathbf{p}_1, \dots, \mathbf{p}_8)$ were stored into the Random Access Memory (RAM) buffers. The indices a in (10) and b in (11) which generated the RAM addresses were easily calculated by the 7-bit accumulators, where $q = 2^7 = 128$. By using an encoding clock frequency of 100 MHz and 912 XOR gates for the additions in (5)-(9), the encoder attained a throughput of 12.8 Gigabit/s.

V. CONCLUSION

This letter has proposed an efficient approach for designing high-performance irregular LDPC codes with low error floor and low encoding complexity. By using techniques such as dual-diagonal matrix decomposition, degree distribution optimization, careful selection of shifting coefficients, and fast estimation of minimum distances, the proposed solutions lower dramatically the BER floor down to 10^{-9} . These techniques are applicable for irregular LDPC codes with arbitrary block length and arbitrary code rate.

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REFERENCES

- [1] R. M. Tanner, D. Sridhara, A. Sridharan, T. E. Fuja, and D. J. Costello, Jr., "LDPC block and convolutional codes based on circulant matrices," *IEEE Trans. Inform. Theory*, vol. 50, pp. 2966-2984, Dec. 2004.
- [2] M. P. C. Fossorier, "Quasi-cyclic low-density parity-check codes from circulant permutation matrices," *IEEE Trans. Inform. Theory*, vol. 50, pp. 1788-1793, Aug. 2004.
- [3] J. Kang, P. Fan, Z. Cao, "Flexible construction of irregular partitioned permutation LDPC codes with low error floors," *IEEE Commun. Lett.*, vol. 9, pp. 534-536, June 2005.
- [4] S. Chung, G. D. Forney, Jr., T. J. Richardson, and R. Urbanke, "On the design of low-density parity-check codes within 0.0045 dB of the Shannon limit," *IEEE Commun. Lett.*, vol. 5, pp. 58-60, Feb. 2001.
- [5] R. Echard and S. Chang, "The extended irregular /spl pi/-rotation LDPC codes," *IEEE Commun. Lett.*, vol. 7, pp. 230-232, May 2003.
- [6] S. J. Johnson and S. R. Weller, "A family of irregular LDPC codes with low encoding complexity," *IEEE Commun. Lett.*, vol. 7, pp.79-81, Feb. 2003.
- [7] T. J. Richardson, M. A. Shokrollahi, and R. L. Urbanke, "Design of capacity-approaching irregular low-density parity-check codes," *IEEE Trans. Inform. Theory*, vol. 47, pp. 619-637, Feb. 2001.
- [8] M. Fossorier and N. Miladinovic, "Irregular LDPC codes as concatenation regular LDPC codes," *IEEE Commun. Lett.*, vol. 9, pp. 628-630, July 2005.
- [9] G. Liva, E. Paolini, and M. Chiani, "Simple reconfigurable low-density parity-check codes," *IEEE Commun. Lett.*, vol. 9, pp. 258-260, Mar. 2005.